STRAINED SILICON-CHANNEL MOSFET USING A DAMASCENE GATE PROCESS

ABSTRACT OF THE DISCLOSURE

The present invention provides a method using a damascene-gate process to improve the transport properties of FETs through strain Si. Changes in mobility and FET characteristics are deliberately made in a Si or silicon-on-insulator (SOI) structure through the introduction of local strain in the channel region, without introducing strain in the device source and drain regions. The method has the advantage of not straining the source and drain regions resulting in very low leakage junctions and also it does not require any special substrate preparation like the case of a strained Si/relaxed SiGe system. Moreover, the method is compatible with existing mainstream CMOS processing. The present invention also provides a CMOS device that has a localized strained Si channel that is formed using the method of the present invention.